UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/709,001	11/08/2000	Matthew B. Haycock	884.302US1	3143

21186 7590 03/29/2004

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
CHANG, ERIC	

ART UNIT	PAPER NUMBER
2116	3

DATE MAILED: 03/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/709,001	HAYCOCK ET AL.	
	Examiner	Art Unit	
	Eric Chang	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23-26* is/are allowed.

6)☒ Claim(s) *1-22 and 27* is/are rejected.

7)☒ Claim(s) *28-30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 November 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 7, 9-10, 13-16, 20-22 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,268,932 to Okuzono.

4. As to claim 1, Okuzono discloses a digital bus comprising:

[a] a transmitter generating a plurality of clock signals [col. 10, lines 47-51];

[b] a receiver comprising one or more FIFO units [col. 11, lines 5-18]; and

[c] a synchronizer receiving the plurality of clock signals, a sample clock signal, and a reset signal and generating a plurality of write reset signals and a read reset signal [FIG. 1, elements 104-105 and 108, col. 6, lines 20-34, col. 10, lines 47-67, and col. 11, lines 1-26];

[d] wherein each of the plurality of reset signals has a latency of less than or equal to a clock cycle with the reset signal [col. 12, lines 8-14]; and

[e] a transmission medium to couple the plurality of clock signals from the transmitter to the receiver [col. 10, lines 47-51].

Okuzono teaches a digital bus receiving a plurality of clock signals from a transmitter, and using a synchronizer to generate a plurality of reset signals to control the flow of data through a plurality of FIFO units based on the plurality of received clock signals and a master sample clock, in order to synchronize the data received over the bus, substantially as claimed.

5. As to claim 2, Okuzono discloses the transmitter comprises a transceiver [FIG. 1, element 101].

6. As to claims 7, 9-10 and 16, Okuzono discloses a transmission line [col. 1, lines 50-53]. It is well known in the art that such a transmission line may comprise any well known means for communicating data from a transmitter to a receiver, such as a cable, metal interconnects, or free space, substantially as claimed.

7. As to claims 13-15, Okuzono discloses a digital bus comprising a transmitter generating a plurality of clock signals, a receiver comprising one or more FIFO units, and a synchronizer receiving the plurality of clock signals, a sample clock signal, and a reset signal and generating a plurality of write reset signals and a read reset signal to synchronize flow of data through the FIFO units, substantially as claimed. Because Okuzono teaches the digital bus, Okuzono teaches an integrated circuit comprising said elements. Furthermore, it is well known in the art that an integrated circuit may be fabricated on a single silicon substrate, substantially as claimed.

8. As to claims 20-22, Okuzono discloses a digital bus comprising a transmitter generating a plurality of clock signals, a receiver comprising one or more FIFO units, and a synchronizer receiving the plurality of clock signals, a sample clock signal, and a reset signal and generating a plurality of write reset signals and a read reset signal to synchronize flow of data through the FIFO units, substantially as claimed. Because Okuzono teaches the digital bus comprising such a synchronizer unit, Okuzono teaches the synchronizer unit. Furthermore, it is well known in the art that a logic circuit may comprise complementary metal-oxide semiconductor logic circuits, and that said circuits have a delay of less than about two nanoseconds, substantially as claimed.

9. As to claim 27, Okuzono discloses a method for synchronizing data from a FIFO using a reset signal based a plurality of clock signals, a master sample clock signal, and a reset signal [col. 6, lines 20-34, col. 10, lines 47-67, and col. 11, lines 1-48]. Okuzono teaches generating an intermediate clock as a synchronized reset signal to reset the plurality of latching means in order to synchronize the data, substantially as claimed.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 3-6, 8, 11-12 and 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,268,932 to Okuzono.

12. As to claim 3, Okuzono discloses the transmitter comprises a transceiver that transfers high bit rate data [FIG. 1, element 101, and col. 1, lines 50-53]. It would have been obvious to one of ordinary skill in the art that the transceiver be any device that transmits and receives high bit rate data, such as a processor, substantially as claimed.

13. As to claims 4-5, Okuzono discloses the phase of one of the plurality of clock signals may be behind the phase of another one of the plurality of clock signals [col. 2, lines 45-53]. It would have been obvious to one of ordinary skill in the art that the phase difference could comprise 180 degrees, or have a skew of less than 90 degrees, or any other difference in phase, substantially as claimed.

14. As to claim 6, Okuzono discloses the transmission medium transfers high bit rate data [col. 1, lines 50-53]. It would have been obvious to one of ordinary skill in the art that data transmitted at 500 MHz to 5 GHz would comprise high bit rate data, substantially as claimed.

15. As to claim 8, Okuzono discloses synchronizing the received clocks with master sample clock [col. 1, lines 59-66]. It would have been obvious to one of ordinary skill in the art that the master clock could be of any rate, such as twice the frequency of the received clocks, substantially as claimed.

16. As to claims 11-12 and 17-19, Okuzono discloses the receiver comprises data terminal equipment that receives high bit rate data [FIG. 1, element 106, and col. 1, lines 50-53]. It would have been obvious to one of ordinary skill in the art that the receiver be any device that receives high bit rate data, such as DRAM or SRAM memory, substantially as claimed.

Allowable Subject Matter

17. Claims 23-26 are allowed.

18. Okuzono, U.S. Patent 5,268,932 teaches a synchronizer receiving the plurality of clock signals, a sample clock signal, and a reset signal and generating a plurality of write reset signals and a read reset signal [FIG. 1, elements 104-105 and 108, and col. 10, lines 47-67, and col. 11, lines 1-26], wherein each of the plurality of reset signals has a latency of less than or equal to a clock cycle with the reset signal [col. 12, lines 8-14].

The prior art of record does not teach or suggest, individually or in combination, a synchronizer comprising: a first, second and third synchronizer unit, or the use of a plurality of serially coupled flip-flops and OR gate in the construction of said synchronizer units, substantially as claimed.

19. Claims 28-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (703) 305-4612. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 15, 2004
ec

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100